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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/783,462	02/20/2004	Ronald Gene Filippi	YOR920040056US1 (163-31)	7450

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EXAMINER	
FULK, STEVEN J	

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 03/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/783,462	FILIPPI ET AL.	
	Examiner	Art Unit	
	Steven J. Fulk	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *06 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16 and 32-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16 and 32-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Non-patent literature*.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment, filed February 6, 2006, which amends claims 1 and 9, cancels claims 17-31, and adds claims 32-25, has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3, 6, 9-11 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by JEDEC Publication JEP139 (PTO-892, Page 1, NPL Reference "U").

JEP139 discloses an industry-standard method for evaluating the reliability of a semiconductor chip structure built by a manufacturing process (page 1, section 1, document describes a constant temperature (isothermal) aging method for...test structures on microelectronics wafers for susceptibility to stress-induced voiding; section 2.1, stress-induced voids in metallization levels cause resistance increases to shorten interconnect lifetime), the method comprising building a via chain test structure in accordance with a manufacturing process used in fabricating a semiconductor chip structure (page 4, section 3.2.1, selecting product wafers containing test structures to sample; page 6, section 3.3.4, multi-level metallization test structures) to test reliability of the semiconductor chip structure, wherein the test structure uses metal and dielectric materials having a mismatch in coefficient of thermal expansion (page 11, section 4.7, difference between the CTE of Al and

the surrounding oxide); and wherein building the test structure provides a uniform stress condition (predetermined strain value) on one or more structures (the difference between the CTE of Al and oxide would inherently provide a uniform, predetermined stress condition);

thermal cycling the test structure to induce changes or failures of the features (page 4, section 3.2.4, baking cycle induces via resistance changes); measuring the yield of the features of the test structure (page 4, section 3.2.4, test readouts), wherein the yield includes a relative number structures formed by the manufacturing process that are electrically active before thermal cycling (page 4, section 3.2.2, initial electrical measurements to ensure structure functionality);

and evaluating the reliability of the semiconductor chip structure built by the manufacturing process based on the yield of the test structure (page 4, section 3.2.5, report failures (read as yield) for each cycle readout; page 5, section 3.2.7, determine metallization lifetime at use conditions from stress data, read as finding use-condition lifetime data of the chip from the test structure stress data).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 4-5, 12-13, 32 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over JEDEC Publication JEP139 in view of Suzuki et al. (PTO-892, Page 1, NPL Reference "V").

a. Regarding claims 4-5 and 12-13, JEP139 discloses all of the elements of the claims as discussed above including building a via chain test structure in accordance with a manufacturing process used in fabricating a semiconductor chip, but the reference does not explicitly disclose building a dual damascene test structure with vias having conductive liners along the bottoms and sidewalls of the vias.

Suzuki et al. teaches a method of measuring the stress-induced void reliability of dual damascene test structures with vias having conductive liners along the bottoms and sidewalls (page 229, "Experimental" section, TaN barrier deposited under the Cu via).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the Cu dual damascene via with a TaN barrier layer of Suzuki et al. as the test structure in the method of JEP139. One would have been motivated to do this because it was well known in the art that the industry-standard metal for interconnects had shifted from aluminum to copper due to the lower resistivity of copper, and it was conventional to form copper interconnects with a barrier layer using a dual damascene process (Suzuki et al., page 229, "Introduction" section).

b. Regarding claims 32 and 34, JEP139 discloses all of the elements of the claims as discussed above including building a via chain test structure in

accordance with a manufacturing process used in fabricating a semiconductor chip, but the reference does not explicitly disclose building vias of a plurality of widths in the test structure.

Suzuki ét al. teaches a method of measuring the stress-induced void reliability of dual damascene test structures with vias having a plurality of widths (page 229, "Experimental" section, vias of varying diameter).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the vias of varying width of Suzuki et al. in the method of JEP139. One would have been motivated to do this because the stress-induced void failure rate of interconnects depends on via width (Suzuki et al., page 229, "Abstract" section). Since semiconductor chips use vias of varying width in their design, one would have been motivated to use a test structure with varying via widths to accurately model the failure rate of the product chip.

6. Claims 7-8 and 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over JEDEC Publication JEP139 in view of Huston et al. (PTO-892, Page 1, NPL Reference "W").

JEP139 discloses all of the elements of the claims as discussed above including building a via chain test structure in accordance with a manufacturing process used in fabricating a semiconductor chip and evaluating the reliability of the semiconductor chip based on the yield of the test structure, but the reference does not explicitly disclose the test structures to have a bimodal failure distribution of

early and late fails during the thermal cycling test, and evaluating the reliability based on the early fails.

Huston et al. teaches a method of reliability defect detection during processing, wherein the yield of a test structure is used to imply the product reliability for chips on the same wafer (page 271, col. 1). The reference discloses that a bimodal failure distribution having early and late fails is inherent in reliability modeling. This is because there are two failure modes during the useful life of a product: extrinsic failure (infant mortality, or early fails due to defects) and intrinsic failure (late fails due to random events). Wear-out is the final failure rate of a product, when it has reached the end of its useful life (page 268, fig. 1).

Huston et al. further defines extrinsic defects in semiconductor chips to include interconnect defects that do not cause a completely open or shorted circuit, but rather "near opens" and "near shorts" that will fail early in the product life (page 269, col. 1-2), meaning failure shortly after it is received by the customer. The reference teaches using the extrinsic fails of test structures to model the reliability of semiconductor chips (page 268, "Abstract" section; page 270, col. 2; extrinsic failure Defect Level (DL) factor is used in the reliability modeling equations).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the extrinsic reliability model of Huston et al. to predict the reliability of the chip in the method of JEP139. One would have been motivated to do this because extrinsic failures are difficult to detect during functional yield

tests (Huston et al., page 269, col. 2), and therefore must be screened by reliability testing to prevent customers from receiving products with high early failure rates.

7. Claims 33 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over JEDEC Publication JEP139 in view of Yao et al. '701.

JEP139 discloses all of the elements of the claims as discussed above including building a via chain test structure in accordance with a manufacturing process used in fabricating a semiconductor, but the reference does not explicitly disclose building the test structure to include a dummy structure to provide a via density in an area of the semiconductor chip structure.

Yao et al. teaches a via chain test structure used for stress-induced void reliability monitoring (col. 1, lines 13-37), wherein the test structure (fig. 1) includes a dummy structure (vias 110) to provide a via density in an area of the semiconductor chip structure (100; col. 3, line 66 – col. 4, line 62).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the dummy structure of Yao et al. in the test structure of JEP139. One would have been motivated to do this because forming a dummy structure to provide via density in an area of the semiconductor chip structure would have made the test structure more sensitive to resistance variation (col. 3, line 66 – col. 4, line 9), thus resulting in a more accurate detection of void formation (resistance shift) in the test structure and improving the reliability model.

Response to Arguments

8. Applicant's arguments with respect to claims 1-16 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Ryan '587 discloses a method of evaluating the thermal stress migration reliability of a semiconductor chip, and teaches that stress migration is the mass transport of interconnect material in response to mechanical stress gradients present in the interconnect which result from thermal expansion coefficient mismatches between the metal layers and surrounding dielectric layers. The reference teaches a method of subjecting a Cu structure with a barrier layer to thermal cycling, determining the void distribution, and using the void data to determine the lifetime (reliability) of the interconnect structure.

b. Fetterman et al. '465, Wang '383 and Werner et al. '901 disclose a Cu dual-damascene test structure with a barrier layer within a semiconductor wafer and method for evaluating stress-induced voids using the test structure, wherein thermal stress is applied and the via resistance shift due to void formation and/or delamination is measured.

c. Langer et al. '786 discloses a Cu dual-damascene test structure with a barrier layer within a semiconductor wafer and method for evaluating stress-induced voids using the test structure, wherein thermal stress is applied and voids are detected with the use of an electron microscope.

d. Fetterman et al. '465 discloses a Cu test structure with a barrier layer within a semiconductor wafer and method for evaluating stress-induced voids

using the test structure, wherein thermal stress is applied and the via resistance shift due to void formation and/or delamination is measured.

e. Graas et al. '181 discloses a via chain test structure within a semiconductor wafer used evaluating stress-induced voids caused by thermal cycling.

f. Chao et al. '350 discloses a method of performing a thermal stress cycle test on a semiconductor chip, and the reference teaches that thermal expansion coefficient mismatch between metals and dielectrics causes metal voiding and film peeling during thermal cycles.

g. Nawa et al. (PTO-892, Page 1, NPL Reference "X") discloses a reliability study for coefficient of thermal expansion mismatching in a semiconductor chip via structure, wherein thermal cycling caused cracks in the interconnects discloses.

h. Ogawa et al. (PTO-892, Page 2, NPL Reference "U") discloses a study of stress-induced voiding in Cu dual-damascene vias with a barrier layer, wherein thermal cycles caused interconnect void failures due to mismatches in thermal expansion coefficients of Cu and the surrounding dielectric.

i. Graas et al. (PTO-892, Page 2, NPL Reference "V") discloses a correlation between via test structure resistance and product reliability, wherein early life failure rate models are used to predict product reliability.

j. Hansen (PTO-892, Page 2, NPL Reference "W") and Papp et al. (PTO-892, Page 2, NPL Reference "X") disclose methods of performing product

reliability monitoring based on wafer-level test structures that are manufactured on the same wafer as product chips.

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven J. Fulk whose telephone number is (571) 272-8323. The examiner can normally be reached on Monday through Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571) 272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Steven J. Fulk
Patent Examiner
Art Unit 2891

BRADLEY K. SMITH
PRIMARY EXAMINER

March 24, 2006